CLAIM AMENDMENTS

1. (original) An inter-device adaptable interfacing clock skewing system, comprising:

a first device; and

a second device that is communicatively coupled to the first device; and

wherein the first device comprises a clock generation circuitry, the clock generation circuitry being operable to select and to provide a clock signal to the second device, the clock signal having a frequency and a phase; and

the first device further comprises a pin that is used to select at least one of the frequency of the clock signal and the phase of the clock signal that is provided to the second device.

2. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the second device selects the pin.

3. (original) The inter-device adaptable interfacing clock skewing system of claim 1, further comprising a register, communicatively coupled to the first device, that comprises information concerning at least one of the phase of the clock signal and the frequency of the clock signal; and

wherein the clock generation circuitry is operable to select and to provide the clock signal to the second device based on the information concerning the at least one of the phase of the clock signal and the frequency of the clock signal within the register.

4. (original) The inter-device adaptable interfacing clock skewing system of claim 3, wherein the register is situated externally with respect to the first device.

5. (original) The inter-device adaptable interfacing clock skewing system of claim 3, wherein the register is contained within the first device.

6. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the first device provides data to the second device.

7. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the first device comprises at least one of a clock generator, a divider, and a delay cell.

8. (original) The inter-device adaptable interfacing clock skewing system of claim 7, wherein an operational parameter of at least one of the clock generator, the divider, and the delay cell is selected using the pin.

9. (original) The inter-device adaptable interfacing clock skewing system of claim 7, wherein the clock generator generates a first clock signal; and

the divider divides down the first clock signal to generate a second clock signal.

10. (original) The inter-device adaptable interfacing clock skewing system of claim 7, wherein the clock generator generates a first clock signal; and

the first clock signal passes through the delay cell and incurs a delay thereby generating a second clock signal, the second clock signal being skewed with respect to the first delay cell.

11. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the first device comprises a phase locked loop that is operable to perform phase shifting of the clock signal before the clock signal is provided to the second device.

12. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the clock signal that is provided from the first device to the second device supports at least one of a 10BaseT protocol, a 100BaseT protocol, and a 1000BaseT protocol.

13. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the first device comprises a multiplexor; and

wherein at least one the frequency of the clock signal and the phase of the clock signal is selected using the multiplexor.

14. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the second devices provides at least one additional clock signal to the first device.

15. (original) The inter-device adaptable interfacing clock skewing system of claim 1, wherein the second devices provides data to the first device.

16. (original) An inter-device adaptable interfacing clock skewing system, comprising:

a first device;

a second device that is communicatively coupled to the first device; and

a register, communicatively coupled to the first device, that comprises information concerning at least one of a phase of a clock signal and a frequency of the clock signal; and

wherein the first device comprises a clock generation circuitry, the clock generation circuitry being operable to select and to provide the clock signal to the second device based on the information concerning the phase of the clock signal and the frequency of the clock signal within the register.

17. (original) The inter-device adaptable interfacing clock skewing system of claim 16, the second device programs the register with the information concerning at least one of the phase of the clock signal and the frequency of the clock signal within the register.

18. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the first device further comprises a pin that is used to select at least one of the frequency of the clock signal and the phase of the clock signal that is provided to the second device.

19. (original) The inter-device adaptable interfacing clock skewing system of claim 18, wherein the second device selects the pin.

20. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the register is situated externally with respect to the first device.

21. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the register is contained within the first device.

22. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the first device provides data to the second device.

23. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the first device comprises at least one of a clock generator, a divider, and a delay cell.

24. (original) The inter-device adaptable interfacing clock skewing system of claim 23, wherein the clock generator generates a first clock signal; and

the divider divides down the first clock signal to generate a second clock signal.

25. (original) The inter-device adaptable interfacing clock skewing system of claim 23, wherein the clock generator generates a first clock signal; and

the first clock signal passes through the delay cell and incurs a delay thereby generating a second clock signal, the second clock signal being skewed with respect to the first delay cell.

26. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the first device comprises a phase locked loop that is operable to perform phase shifting of the clock signal before the clock signal is provided to the second device.

27. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the clock signal that is provided from the first device to the second device support at least one of a 10BaseT protocol, a 100BaseT protocol, and a 1000BaseT protocol.

28. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the first device comprises a multiplexor; and

wherein at least one the frequency of the clock signal and the phase of the clock signal is selected using the multiplexor.

29. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the second devices provides at least one additional clock signal to the first device.

30. (original) The inter-device adaptable interfacing clock skewing system of claim 16, wherein the second devices provides data to the first device.

31. (original) An inter-device adaptable interfacing clock skewing method, the method comprising:

skewing a first clock signal to generate a second clock signal, the second clock signal having a phase difference with respect to the first clock signal, the skewing of the first clock signal being performed within a first device; and

communicating the second clock signal from the first device to a second device; and

wherein the second clock signal comprises a frequency and a phase.

32. (original) The method of claim 31, wherein the phase difference substantially comprises at least one of zero degrees and ninety degrees.

33. (original) The method of claim 31, wherein the first device receives the first clock signal.

34. (original) The method of claim 31, wherein the first device generates the first clock signal.

35. (original) The method of claim 31, further comprising dividing down the first clock signal to generate the second clock signal.

36. (original) The method of claim 31, further comprising selecting at least one of the frequency of the second clock signal and the phase of the second clock signal using information contained within a register.

37. (original) The method of claim 36, wherein the second device programs the register.

38. (original) The method of claim 36, wherein the register is situated externally with respect to the first device.

39. (original) The method of claim 36, wherein the register is contained within the first device.

40. (original) The method of claim 31, further comprising selecting at least one of the frequency of the clock signal and the phase of the second clock signal using a pin.

41. (original) The method of claim 40, wherein the second device selects the pin.

42. (original) The method of claim 31, wherein the second clock signal supports at least one of a 10BaseT protocol, a 100BaseT protocol, and a 1000BaseT protocol.

43. (original) The method of claim 31, further comprising employing a phase locked loop to perform the skewing the first clock signal to generate the second clock signal.

44. (original) The method of claim 31, further comprising communicating data between the first device and the second device.

45. (currently amended) An inter-device adaptable interfacing clock skewing method, the method comprising:

skewing a phase of a ~~the~~ first clock signal and dividing down a frequency of the first clock signal to generate a second clock signal;

generating a second clock signal within a first device, the second clock signal having a phase difference with respect to the first clock signal and a divided down frequency with respect to the first clock signal; and

communicating the second clock signal from the first device to a second device; and

wherein the second clock signal comprises a frequency and a phase.

46. (original) The method of claim 45, further comprising generating the first clock signal within the first device.

47. (original) The method of claim 45, further comprising receiving the first clock signal into the first device.

48. (original) The method of claim 45, further comprising selecting at least one of the frequency of the second clock signal and the phase of the second clock signal using at least one of a pin and information contained within a register.

49. (original) The method of claim 48, further comprising programming the register using the second device.

50. (original) The method of claim 45, wherein the second clock signal supports at least one of a 10BaseT protocol, a 100BaseT protocol, and a 1000BaseT protocol.

51. (currently amended) An inter-device adaptable interfacing clock skewing system, comprising:

a first device that provides a clock signal; and

a second device, ~~is~~ communicatively coupled to the first device, that receives the clock signal; and

wherein the second device comprises a clock skewing circuitry, the clock skewing circuitry being operable to skew the received clock signal to generate a skewed clock signal, the skewed clock signal having a frequency and a phase; and

the second device further comprises a pin that is used to select at least one of the frequency of the skewed clock signal and the phase of the skewed clock signal that is generated within the second device.

52. (original) The inter-device adaptable interfacing clock skewing system of claim 51, wherein the first device selects the pin.

53. (original) The inter-device adaptable interfacing clock skewing system of claim 51, further comprising a register, communicatively coupled to the second device, that comprises information concerning at least one of a phase of a clock signal and a frequency of a clock signal; and

wherein the clock skewing circuitry is operable to divide and delay the received clock signal to generate the skewed clock signal based on the information concerning at least one of the phase of the clock signal and the frequency of the clock signal within the register.

54. (original) The inter-device adaptable interfacing clock skewing system of claim 53, wherein the register is situated externally with respect to the second device.

55. (original) The inter-device adaptable interfacing clock skewing system of claim 53, wherein the register is contained within the second device.

56. (original) The inter-device adaptable interfacing clock skewing system of claim 51, wherein the first device provides data to the second device.

57. (original) The inter-device adaptable interfacing clock skewing system of claim 51, wherein the second device comprises at least one of a divider and a delay cell.

58. (original) The inter-device adaptable interfacing clock skewing system of claim 57, wherein an operational parameter of at least one of the divider and the delay cell is selected using the pin.

59. (original) The inter-device adaptable interfacing clock skewing system of claim 57, wherein the clock skewing circuitry divides down the received clock signal to generate the skewed clock signal.

60. (original) The inter-device adaptable interfacing clock skewing system of claim 57, wherein the clock skewing circuitry passes the received clock signal through a delay cell to incur a delay thereby generating the skewed clock.

61. (original) The inter-device adaptable interfacing clock skewing system of claim 51, wherein the second device comprises a phase locked loop that is operable to perform phase shifting of the received clock signal.

62. (original) The inter-device adaptable interfacing clock skewing system of claim 51, wherein the clock signal that is provided from the first device to the second device supports at least one of a 10BaseT protocol, a 100BaseT protocol, and a 1000BaseT protocol.

63. (original) An inter-device adaptable interfacing clock skewing method, the method comprising:

transmitting a clock signal from a first device;

receiving the clock signal in a second device, the clock signal received by the second device comprising a received clock signal; and

skewing the received clock signal within the second device to generate a skewed clock signal, the skewed clock signal having a phase difference with respect to the received clock signal; and

wherein the skewed clock signal comprises a frequency and a phase.

64. (original) The method of claim 63, wherein the phase difference substantially comprises at least one of zero degrees and ninety degrees.

65. (original) The method of claim 63, further comprising dividing down the received clock signal to generate the skewed clock signal.

66. (original) The method of claim 63, further comprising selecting at least one of the frequency of the skewed clock signal and the phase of the skewed clock signal using information contained within a register.

67. (original) The method of claim 66, wherein the first device programs the register.

68. (original) The method of claim 66, wherein the register is situated externally with respect to the second device.

69. (original) The method of claim 66, wherein the register is contained within the second device.

70. (original) The method of claim 63, further comprising selecting at least one of the frequency of the skewed clock signal and the phase of the skewed clock signal using a pin.

71. (original) The method of claim 70, further comprising programming the pin using the first device.

72. (original) The method of claim 63, wherein the skewed clock signal supports at least one of a 10BaseT protocol, a 100BaseT protocol, and a 1000BaseT protocol.

73. (original) The method of claim 63, further comprising employing a phase locked loop to perform the skewing the received clock signal to generate the skewed clock signal.

74. (original) The method of claim 63, further comprising communicating data between the first device and the second device.

75. (original) An inter-device adaptable interfacing clock skewing system, comprising:

a first device that comprises a clock generation circuitry; and

a second device, communicatively coupled to the first device, that comprises a clock skewing circuitry; and

wherein clock generation circuitry being operable to select and to provide a transmitted clock signal from the first device to the second device, the transmitted clock signal having a transmitted frequency and a transmitted phase;

the second device comprises a clock skewing circuitry, the clock skewing circuitry being operable to skew a received clock signal to generate a skewed clock signal, the received clock signal being transmitted by the first device and received by the second device and the skewed clock signal having a received frequency and a received phase;

the first device further comprises a first pin that is used to select at least one of the frequency of the transmitted clock signal and the phase of the transmitted clock signal that is provided from the first device to the second device; and

the second device further comprises a second pin that is used to select at least one of the frequency of the skewed clock signal and the phase of the skewed clock signal that is generated within the second device.

76. (original) An inter-device adaptable interfacing clock skewing system, comprising:

a first device that comprises a clock generation circuitry that is operable to ;

a second device, communicatively coupled to the first device, that comprises a clock skewing circuitry; and

a first register, communicatively coupled to the first device, that comprises information concerning at least one of a phase of a transmitted clock signal and a frequency of the transmitted clock signal;

a second register, communicatively coupled to the second device, that comprises information concerning at least one of a phase of a received clock signal and a frequency of the received clock signal; and

wherein the clock generation circuitry is operable to select and to provide the transmitted clock signal to the second device based on the information concerning at least one of the phase of the transmitted clock signal and the frequency of the transmitted clock signal within the first register;

the clock skewing circuitry is operable to skew the received clock signal to generate a skewed clock signal based on the information concerning at least one of the phase of the received clock signal and the frequency of the received clock signal within the second register.